REMARKS

The following remarks are deemed fully responsive to the office action mailed June 3, 2005. Claim 4 is amended to correct antecedence. Claim 5 is amended for clarity. Claim 9 is amended to correct a spelling mistake. No new matter is added. Claims 1 – 20 remain pending, of which claims 1, 11, 19 and 20 are independent.

Claim Rejections – 35 U.S.C. § 112

Claim 5 stands rejected for being unclear under 35 U.S.C. §112, second paragraph. We have amended this claim and believe that amended claim 5 obviates the present rejection. Reconsideration is requested.

Claim Rejections – 35 U.S.C. § 103

When applying 35 U.S.C. §103, the following tenets of patent law must be adhered to:

a) The claimed invention must be considered as a whole;
b) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination;
c) The references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and
d) Reasonable expectation of success is the standard with which obviousness is determined. MPEP §2141.01, *Hodosh v. Block Drug Co., Inc.*, 786 F.2d 1136, 1134 n.5, 229 U.S.P.Q. 182, 187 n.5 (Fed. Cir. 1986).

In addition, it is respectfully noted that to substantiate a *prima facie* case of obviousness the initial burden rests with the Examiner who must fulfill three requirements. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable

expectation of success must both be found in the prior art, and not based on Applicant's disclosure. (emphasis and formatting added) MPEP § 2143, *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Claims 1, 3-7, 10, 19 and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Number 6,848,100 granted to Wu et al. (hereinafter "Wu"). Respectfully we disagree.

The immediate application teaches a processor with two or more parallel instruction paths that process instructions; the instruction paths may be implemented as a programming core within an EPIC processor, and on a common die. See paragraph [0019]. FIG. 1 of the immediate application for example shows an architecture 10 with an array of execution paths 12(1-N) that process instructions through execution units 14(1-N), respectively. Each of the instruction paths 12 has an array of pipelined execution units 14. Two or more parallel instruction paths process the same program thread with different optimization characteristics. Assessment logic monitors the processing of the initial program thread and selects heuristics defining which path is in the lead. The lead path continues processing the initial thread without being disturbed and the other paths are reallocated, or synchronized, with the optimization characteristics of the lead instruction path. See paragraph [0007] of the immediate specification.

On the other hand, Wu discloses a hierarchical ***software*** profiling mechanism that provides profiling information to optimizing compilers. See Wu col. 1, lines 19-20. More specifically, Wu modifies software to sum edge values along paths as they are executed. Wu does not disclose processing of instructions through a processor with at least two parallel instruction processing paths and associated heuristics affecting how the instructions are processed. The software paths of Wu **are not** equivalent to the processing paths of the processor of the immediate application. Wu specifically pertains to code optimization, as opposed to processor optimization as taught by the immediate application and claims. The profile characteristics of Wu **are not** equivalent to heuristics of the immediate application. Wu does not teach or suggest optimizing characteristics of a processor.

In fact, Wu teaches away from the immediate application because Wu modifies software by inserting profiling instructions, thereby reducing execution

performance of the software. Wu is therefore non-analogous to performance optimization of multi-core processors as in the present claims. Further, the profiling information output by Wu's hierarchical software profiling mechanism is not suitable for optimizing characteristics of a processor.

Referring now to the claims, claim 1 recites a method for optimizing the processing of instructions through a processor, including the steps:

a) processing first like instructions through two or more instructions paths of the processor, each of the paths having different heuristics associated therewith;
b) monitoring progress of the first like instructions through the instruction paths;
c) determining which of the instruction paths is a first leader in processing the first like instructions; and
d) modifying heuristics of one or more of the instruction paths based on heuristics of the first leader.

As noted above, Wu does not disclose a method that optimizes the processing of instructions through a processor. Wu does not, for example, disclose or suggest (a) processing of instructions through two or more instruction paths, (b) determining which of the instruction paths is a first leader, or (c) modifying heuristics of one or more of the instruction paths. Further, since the information produced by the mechanism of Wu pertains to software profiling, and hence software optimization, it is obviously of no benefit in optimizing characteristics of a processor to improve processor performance.

For at least these reasons, Wu cannot render claim 1 obvious.

Claims 3-7 and 10 depend from claim 1 and benefit from like argument. However, these claims have other features that patentably distinguish over Wu. For example, claim 3 recites modifying heuristics of each of the instruction paths. Claim 4 recites modifying heuristics of instruction paths other than heuristics of the first leader. Wu does not disclose or suggest modifying heuristics of instruction paths within the processor and, therefore, cannot render claims 3 and 4 obvious.

Claim 5 recites processing the first like instructions through the first leader while being unaffected by modified heuristics. Claim 6 recites processing additional instructions from a program thread of the first like instructions through the multiple instruction paths and without redundancy. Claim 7 recites processing second like

instructions through two or more instructions paths of the processor, each of the paths having different heuristics associated therewith, monitoring progress of the second like instructions through the instruction paths, determining which of the instruction paths is a second leader in processing the instructions, and modifying heuristics of one or more of the instruction paths based on heuristics of the second leader. As above, Wu does not disclose or suggest multiple instruction paths within a processor or of modifying heuristics thereof and therefore cannot render claims 5-7 obvious.

Claim 10 recites asymptotically approaching optimized characteristics for the instruction paths. Wu does not disclose or suggest asymptotically approaching optimized characteristics for the instruction paths and therefore, Wu cannot render claim 10 obvious.

Claim 19 recites a processor of the type having at least two parallel instruction paths, each of the paths having an array of pipeline execution units and associated heuristics affecting how the instructions are processed, the improvement including assessment logic for monitoring processing of the instructions within the paths and for modifying the heuristics of at least one of the paths to improve per thread performance of the processor. As argued above, Wu does not disclose or suggest a processor of the type having at least two parallel instruction paths. Further, Wu does not disclose that each of the paths have an array of pipeline execution units with associated heuristics that affect how the instructions are processed. Wu does not disclose or suggest assessment logic for monitoring processing of the instructions within the instruction paths and for modifying the heuristics of at least one of the instruction paths to improve per thread performance of the processor. Clearly, Wu cannot render claim 19 obvious.

Claim 20 depends from claims 19 and benefits from like argument. Claim 20 also recites the further improvement wherein the parallel instruction paths are constructed and arranged to initially process first like instructions therethrough, the assessment logic monitoring the processing of the first like instructions to determine optimized heuristics for the instruction paths. Again, Wu does not address monitoring of instruction processing within instruction paths to determine optimized heuristics for the instruction paths, and cannot therefore render claim 20 obvious.

Reconsideration and allowance of claims 1, 3-7, 10, 19 and 20 is respectfully requested.

Claims 2, 8 and 9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Wu in view of U.S. Patent Number 6,658,447 granted to Cota-Robles (hereinafter "Cota-Robles"). Respectfully we disagree.

Claim 2 depends from claim 1 and thus the arguments for claim 1 also apply to claim 2. In particular, claim 2 recites grouping the first like instructions as a bundle from a common program thread. On the other hand, Cota-Robles discloses a simultaneous multithreading ("SMT") processor architecture that combines thread execution heuristics with operating system priorities to provide a dynamic priority for each thread scheduled on an SMT processor. See Cota-Robles col. 2, lines 55-18. Cota-Robles does not disclose or suggest a processor with at least two parallel instruction processing paths and associated heuristics that affect how the instructions are processed, as required by claim 1. Cota-Robles states that "heuristics are criteria, such as per thread counts of selected events, that are employed by an SMT processor to determine, for example, the efficiency with which a thread is being executed." See Cota-Robles col. 4, lines 15-19. Since Cota-Robles does not disclose a processor with two or more instruction paths, Cota-Robles cannot disclose steps of claim 1, namely: i) processing like instructions through two or more instruction paths, ii) determining which of the instruction paths is a first leader, or iii) modifying heuristics of one or more of the instruction paths based on heuristics of the first leader. In fact, Cota-Robles does not disclose or suggest, anywhere, **modification** of heuristics to improve thread throughput. Further, Cota-Robles recites "the processor fetches a selected number of instructions from among the scheduled threads on a rotating basis," Cota-Robles col. 4, lines 26-28; this teaches away from claim 2, which requires grouping like instructions as a bundle from a **common** program thread. Cota-Robles and Wu therefore cannot render claim 2 obvious.

Claim 8 depends from claim 1 and recites modifying one or more of CPU-bound heuristics and memory-bound heuristics. Claim 9 depends from claim 1 and recites modifying heuristics based upon one or more of branch prediction and prefetch heuristics. Cota-Robles, as argued above, does not disclose or suggest modification of

heuristics to improve thread throughput and cannot therefore render claims 8 and 9 obvious. Thus Wu and Cota-Robles cannot render claims 2, 8, 9 obvious.

Reconsideration of claims 2, 8 and 9 is respectfully requested.

Claims 11, 13-16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Wu in view of U.S. Patent Number 5,909,565 granted to Morikawa et al. (hereinafter "Morikawa").

Claim 11 recites a processor for processing program instructions, including:

a) at least two parallel instruction paths, each of the paths having an array of pipeline execution units and associated heuristics affecting how the instructions are processed therein; and

b) assessment logic for monitoring processing of the instructions within the paths and for modifying the heuristics of at least one of the paths to improve per thread performance of the processor.

As argued above, Wu does not disclose or suggest a processor for processing program instructions and having at least two parallel instruction paths. Morikawa's disclosure (FIG. 1) two data processing units still does not disclose or suggest two parallel instruction paths, as in claim 11 and shown in FIG. 1 of the immediate application. For instance, FIG. 1 of the present application clearly shows each processing path with an instruction cache 22, fetch heuristics 24, instruction issue section 26, execution heuristics 28, execution units 14 and data cache 30 with cache heuristics 32. The two data processing units of Morikawa are **not** equivalent to the instruction paths of the immediate application (and claim 11). Further, Morikawa also fails to disclose or suggest modification of processor heuristics to optimize instruction processing. Therefore, Morikawa fails to overcome the shortcomings of Wu. At least for these reasons, Wu in view of Morikawa cannot render claim 11 obvious.

Claims 12, 17 and 18 stand rejected under U.S.C. 35 § 103(a) as being unpatentable over Wu and Morikawa as applied to claim 11, and further in view of Cota-Robles. As argued above, Wu in view of Morikawa cannot render claim 11 obvious, and like argument applies to claims 12, 17 and 18 that depend from claim 11. Further, since Cota-Robles does not disclose or suggest modification of heuristics to improve per-thread performance of the processor, as required by claim 11, Cota-

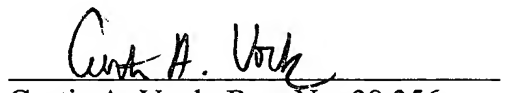
Robles does not overcome the short-fall of Wu and Morikawa in rendering claim 11 obvious.

Moreover, claim 12 recites the heuristics of each of the instruction paths having one or more of fetch heuristics, execution heuristics, and cache heuristics. Claim 17 recites each of the parallel instruction paths forming a cluster constructed and arranged to process instructions as bundles. Claim 18 recites the parallel instruction paths and assessment logic cooperating to process one or more bundles of like instructions through the instruction paths to monitor and then modify heuristics of the instruction paths to improve per thread processing of the instructions. Clearly, each of claims 12, 17 and 18 require multiple instruction paths as shown in FIG. 1 of the immediate specification. The combination of Wu, Morikawa and Cota-Robles does not disclose such instruction paths. Wu, Morikawa and Cota-Robles also do not disclose processing bundles of like instructions through the instruction paths to monitor and then modify heuristics of the instruction paths, as required by claim 18. Wu, Morikawa and Cota-Robles, even when combined, cannot therefore render claims 12, 17 and 18 obvious.

Reconsideration of claims 12, 17 and 18 is respectfully considered.

Applicant believes no fees are due in connection with this Amendment and Response; however, if any fee is deemed necessary, the Commissioner is authorized to charge such fee to Deposit Account No. 08-2025.

Respectfully submitted,

By: 

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